JOINT OPERATIONAL PROBLEM · CONTESTED LOGISTICS · TACTICAL POWER RESILIENCE

WHEN THE BATTERY DIES, THE MISSION DIES. UNLESS SENTINEL IS THERE.

A hardware-immutable power protection and autonomous recovery device that eliminates battery-induced mission failure at the tactical edge — with zero depot access, zero software vulnerability, and zero personnel required.

THE OPERATIONAL PROBLEM

A single BMS fault code can render a $4,000 battery permanently inoperable — with no autonomous recovery path.

Every MIL-PRF-32565C Li-ion 6T battery in the Army's fleet relies on a software-defined Battery Management System for protection. When a fault occurs — even a harmless transient voltage spike — the BMS enters a permanent **Protected State lockout**. In a garrison environment, a depot technician clears the code. In a contested environment, no technician exists. After 24 hours, the battery enters an irreversible Dormant State and begins permanent self-discharge.

29%
FLEET PREMATURE DISPOSAL RATE FROM SOFTWARE LOCKOUTS

$100M
ANNUAL PREVENTABLE LOGISTICS WASTE, ARMY-WIDE

↓ CONTESTED LOGISTICS FAILURE CHAIN

01 Transient arc fault or inductive spike occurs on FOB microgrid
02 BMS software registers fault → Protected State lockout
03 No depot technician available → fault code not cleared
04 24 hours: Dormant State → battery begins permanent self-discharge
05 Battery is bricked. Power is lost. Asset requires resupply.

In a contested, comms-degraded, or austere environment — resupply is not an option. The battery must recover itself.

THE SENTINEL SOLUTION

SENTINEL V2.5 TACTICAL

A potted inline interceptor mounting between the 6T battery terminals and the load. Retrofits any existing MIL-PRF-32565C battery regardless of age, vendor, or chemistry. No modification to the battery. No software. No network dependency.

HARDWARE VETO CORE — < 10µs
An instruction-less Finite State Machine — no OS, no firmware — physically severs fault current in under 10 microseconds. Acts before the BMS can register the fault. Eliminates Protected State entry entirely for transient events. Immune to cyber attack: no software attack surface exists.

LAZARUS PROTOCOL — Autonomous
For faults that do cause a BMS lockout, Sentinel autonomously issues the J1939 CAN "Reset Protection" command — the officially defined maintenance interface in MIL-PRF-32565C §3.6.6.5. Battery returns to Ready state. No soldier. No technician. No radio call for support.

ARGOS EDGE AI — 500 kHz
Digital signal processing analysis at 500 kHz captures electrochemical degradation signatures — dendrite growth, lithium plating — weeks before electrical failure. Predictive maintenance intelligence delivered at the battery terminal, fully offline, in comms-denied environments. No cloud dependency.

48V ARRAY MANAGEMENT — Multi-battery
Enables safe series/parallel combination of 6T batteries of mixed ages, vendors, and chemistries on 48VDC tactical microgrids. Autonomously isolates a failing battery from the bus — preventing cascade failure across the entire array.

WHY ONLY SENTINEL

- ☑ **RETROFIT — NO NEW BATTERY REQUIRED**
  Works on the fleet that exists today. Every competing approach requires a new BMS, a new battery, or rack-level hardware. Sentinel attaches inline in minutes.
- ☑ **ZERO NETWORK DEPENDENCY**
  All intelligence runs on-device. No cloud. No radio. No connectivity required. Sentinel operates in fully comms-denied, GPS-denied, and electromagnetically contested environments.
- ☑ **CYBER-IMMUNE BY ARCHITECTURE**
  No operating system. No firmware. No software update path. The safety logic is etched into non-volatile FPGA configuration memory. It cannot be hacked, patched, or corrupted.
- ☑ **BATTLE OVERRIDE PRIMARY SAFETY LAYER**
  When BMS software protections are intentionally reduced in Battle Override mode (MIL-PRF-32565C §3.3.6), Sentinel's hardware veto becomes the primary — and only — active safety layer on the battery.
- ☑ **TRIPLE MODULAR REDUNDANCY**
  Safety logic runs across three parallel FPGA cores with majority-vote arbitration. Immune to EMI, neutron flux, and shock/vibration-induced false disconnects in kinetic environments.

PROGRAM STATUS & ACQUISITION PATH

PHASE I	● **Under Army Evaluation** — SBIR Topic A254-P050. $249K, 6-month feasibility. SPICE validation, FPGA HIL demo, ARGOS AI mathematical proof.
PHASE II	Ruggedized mixed-signal PCB prototype. MIL-STD-461/810 environmental hardening. Depot and FOB integration testing.
PHASE III	OTA → Low-Rate Initial Production. IP licensing to Tier-1 BMS vendors. Sole-source SBIR Phase III contract.
DIU / OTA	Available for Contested Logistics portfolio engagement via Vulcan. Parallel track to SBIR. Open to CSO, OTA prototype, or rapid fielding vehicle.

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Engineering Partner: BLT, Inc. (Columbia, MD)
Lattice Authorized Design Partner · ITAR / CMMC / DCAA Compliant · Navy Tier-1 Prime

HUBZONE LOCATED